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Hanson Liu

Analog/Mixed-Signal/RFIC design

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About Me

Master's student with a passion for ***High-Speed/SerDes*** and ***Mixed-Signal*** design, with design and tape-out experience in **TSMC 65nm**, **GF 65nm FD-SOI**, and **IBM 180nm** process nodes. Seeking an analog, mixed-signal, or RF integrated circuit design internship/full-time role.

Work Experience

RFIC Design Intern – pSemi, A Murata Company **July 2025 – Present**
San Diego, CA

- Improved power handling and isolation of RF switch products in GF 65nm FD-SOI through design optimization.
- Automated system-level measurements (P0.1dB, IP3, power derating) via custom Ocean scripts in Cadence Spectre/SKILL.
- Measured S-parameters, IP3, P0.1dB compression, and thermal resistivity on evaluation boards of in-development RF switch products.

Application Engineering Intern – Analog Devices **June 2024 – September 2024**
Chandler, AZ

- Developed an SMD revision of an ADI AC ripple-injection lab board (up to 10MHz) in Cadence Allegro.
- Simulated the revised ripple injection board in LTSpice to verify functionality and closed-loop stability.
- Conducted PSRR lab measurements on new lines of ADI low-dropout regulators and step-down buck regulators.

Teaching Assistant – UCSD ECE Department **July 2023 – Present**
San Diego, CA

- Mentored students in CMOS mixed-signal design, control theory, circuits, and systems analysis across 8 quarters and 5 courses.

Projects

Delta-Length SAR ADC with Boot-Strapped Switches Tapeout (TSMC 65nm) **June 2026**

- Designed and laid out a 9-bit SAR ADC in TSMC 65 nm featuring a unit-via based delta-length CDAC, bootstrapped sampling switches with deep-N-well devices, and a monotonic top-plate sampling switching algorithm.
- Achieved a post-extraction simulated 49.1 dB SNDR at just 120 $\mu\mathrm{W}$ and a 143 $\mu\mathrm{m} \times 74\ \mu\mathrm{m}$ total area — the lowest power and smallest area in the class — alongside a dynamic two-stage comparator with $\sim$700 $\mu\mathrm{V}$ mean offset and heavily optimized input capacitance.
- Selected to present design and layout to Apple Cohorts during weekly design review

High-Speed PAM-2 and PAM-4 Voltage-Mode Hybrid Transmitter (TSMC 65nm) **March 2026**

- Designed a voltage-mode driver implementing auxiliary push/pull current-mode logic swing enhancement; achieved simulated data rates of **18Gbps** at 3pJ/bit for PAM-2 and **22Gbps** at 0.68pJ/bit for PAM-4 using a physically measured lossy channel model.
- Satisfied receiver input eye height and aperture margin at a BER of 10^{-12} under additive noise and jitter.
- Implemented 4-tap feed-forward equalization, high-speed level shifters, and digitally controlled tunable termination.

PAM-2 12Gbps Receiver with CTLE and 2-Tap DFE (TSMC 65nm) **March 2026**

- Designed a broadband receiver with a simulated data rate of **12Gbps** using a physically measured lossy channel model.
- Implemented 2-tap decision feedback equalization, a high-sampling-bandwidth StrongARM latch comparator, and an analog front end with a Continuous-Time Linear Equalizer stage and shunt active inductive peaking network for channel bandwidth extension.

Robust Ultra-Low-Power Electrocardiogram Instrumentation Amplifier (IBM 180nm) **December 2025**

- Designed an ECG instrumentation amplifier with a driven-right-leg circuit, achieving nominal power consumption of **667nW** and total integrated input-referred noise of 2.76μVrms, outperforming the required 4μW power specification.
- Ran Monte Carlo mismatch analysis at TT/SS/FF PVT corners, verifying CMRR, gain, bandwidth, and noise was PVT robust across 3σ.

Folded Cascode Operational Transconductance Amplifier (IBM 180nm) **November 2024**

- Designed a high-gain differential OTA and its respective biasing network in Cadence Virtuoso. Achieved a simulated nominal gain of 83.5dB and 30MHz unity-gain bandwidth.
- Presented the design using gm/ID methodology to Apple Cohorts in an end-of-quarter competition; ranked 2nd lowest in power consumption out of 150+ students with **66μW** versus a class mean of $\sim$**1100μW**.

Education

University of California, San Diego **Jacobs School of Engineering**
B.S. in Electrical Engineering *Graduated June 2025,* ***GPA: 3.72/4.0***
M.S. in Electronic Circuits and Systems *Expected Graduation December 2026,* ***GPA: 3.82/4.0***

Technical Skills

Languages	C, C++, SKILL, Verilog, MATLAB
Software	Cadence Spectre, Cadence Virtuoso, Cadence Layout Suite, Cadence Allegro, LTSpice, PSpice/CaptureCIS, HFSS, Maxwell 3D, SIWave, ADS, KiCAD, Vivado, Fusion360
Physical	Spectrum Analyzer, VNA, Oscilloscope, Soldering (SMD & THT), System Debugging, Prototyping